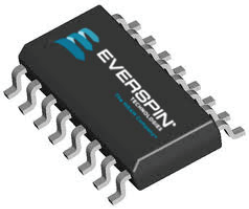
SOIC PACKAGE



16-pin SOIC

- Compliant with RoHS, REACH regulations and practices.
- Contain no Red Phosphorus.
- Lead Free.
- All products meet MSL-3 moisture sensitivity level.
- Standard Reflow profile.
- Compatible with similar low-power SRAM products and other nonvolatile RAM products.

TABLE OF CONTENTS

COMPLIANCE WITH ENVIRONMENTAL REGULATIONS AND DIRECTIVES 2

Table 1 – Environmental Regulation and Directive Compliance 2

MULTIPLE REFLOW CYCLES AND MOISTURE RESISTANCE 2

RECOMMENDED REFLOW TEMPERATURES AND TIMING 3

Figure 1 – JEDEC J-STD-020D.1 Assembly Reflow Profile 3

Table 2 – Recommended Reflow Times and Temperatures - All Packages 3

THERMAL RESISTANCE 4

Table 3 – Thermal Resistance 16-pin SOIC 4

PACKAGE OUTLINE DRAWINGS 5

Figure 2 – Package Outline 16-pin SOIC 5

REVISION HISTORY 6

CONTACT US 7

COMPLIANCE WITH ENVIRONMENTAL REGULATIONS AND DIRECTIVES

Table 1 – Environmental Regulation and Directive Compliance

Environment	Statement Summary	Download Full Statement
ISO9001:2008	Everspin Technologies is in conformance with ISO9001:2008	Certificate
RoHS Directives	Statement of RoHS 1 and the recast Directive 2011/65/EU is commonly referred to as RoHS 2 Compliance. Everspin MRAM products are also "halogen-free".	Full Statement
REACH Regulations	REACH regulations require article suppliers to inform recipients if an article contains a Substance of Very High Concern (SVHC) in excess of 0.1% by weight. Based on the material content certifications provided by Everspin's suppliers, none of these substances are present in the materials we use in our products, including packing and shipping materials.	Full Statement
Red Phosphorus	Everspin Technologies, Inc. MRAM products do not contain Red Phosphorus CAS# 7723-14-0 as an intentional additive.	Full Statement

MULTIPLE REFLOW CYCLES AND MOISTURE RESISTANCE

All Everspin packages are qualified by the procedure defined in IPC/JEDEC joint specification IPC/JEDEC J-STD-020D.1. They are guaranteed to withstand up to three reflow cycles without permanent damage, provided the conditions for the rated moisture resistance level for the part are observed prior to reflow.

Everspin parts are generally rated for MSL Level 3. Exceptions may exist and are noted in their respective data sheet. Please the check the latest individual product data sheet to confirm the rated MSL for the product.

RECOMMENDED REFLOW TEMPERATURES AND TIMING

Everspin products can be assembled using a standard assembly lead-free reflow profile. The profile below is based on IPC/JEDEC J-STD-020D.1.

Figure 1 – JEDEC J-STD-020D.1 Assembly Reflow Profile

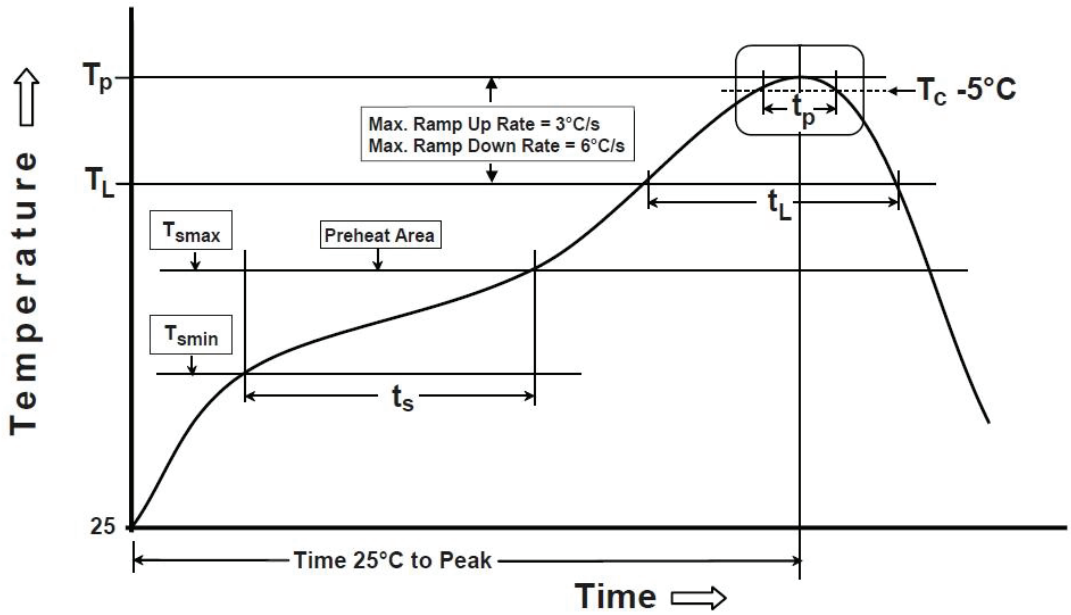


Table 2 – Recommended Reflow Times and Temperatures - All Packages

Profile Step	Parameter	Symbol	Time/Temp	Unit
Preheat / Soak	Temperature mininumum	T_{SMIN}	150	°C
	Temperature maximum	T_{SMAX}	200	°C
	Soak Time	t_S	60 - 120	Seconds
Ramp Up	Rate from T_L to T_P	T_L to T_P	3° / Sec Max	° / Sec
	25°C to T_P		8 minutes max	Minutes
Reflow	Liquidous Temperature	T_L	217	°C
	Time Above T_L		60 - 150	Seconds
	Peak Package Body Tempera-ture	T_P	260	°C
	Time within 5° of Peak Package Body Temperature		20 - 40	Seconds
Ramp Down	Rate from T_P to T_L	T_P to T_L	6° / Sec Max	° / Sec

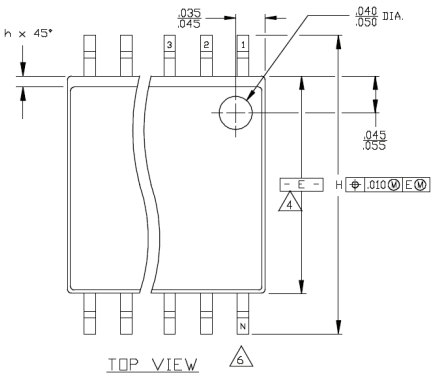
THERMAL RESISTANCE

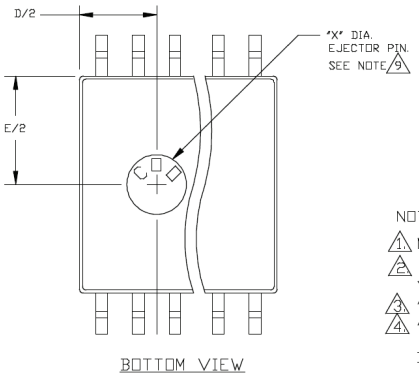
Table 3 – Thermal Resistance 16-pin SOIC

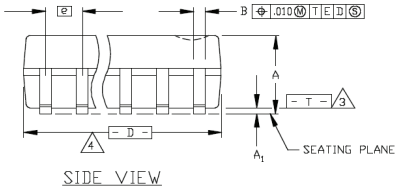
Velocity (m/s)	T_A (°C)	Power (W)	T_J Max °C	Θ_{JA} (°C/W)	Θ_{JB} (°C/W)	Θ_{JC} (°C/W)	Ψ_{JB} (°C/W)	Θ_{JT} (°C/W)
0	25	0.792	71.0	58.1	30.6	31.6	2.0	30.6
1			64.5	49.9			2.8	29.6
2			62.8	47.7			3.2	29.1
3			61.8	46.4			3.5	28.8

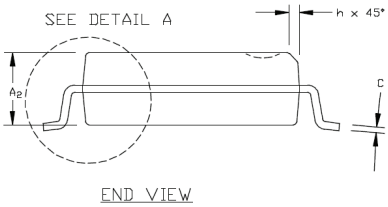
PACKAGE OUTLINE DRAWINGS

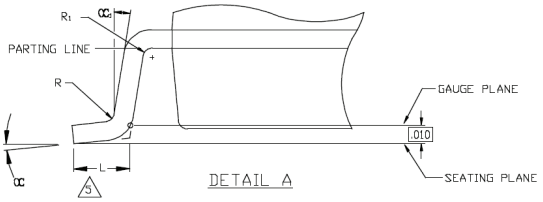
Figure 2 – Package Outline 16-pin SOIC











NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .025.
2. DIMENSIONING & TOLERANCES PER ANSI. Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES AT END AND .010 INCHES AT WINDOW.
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. COUNTRY OF ORIGIN LOCATION ON PACKAGE BOTTOM IS OPTIONAL AND DEPENDS ON ASSEMBLY LOCATION. "KOREA" FOR AICL AND "PHILIPPINES" FOR AAP1.
10. CONTROLLING DIMENSION: INCHES.
11. THIS PART IS COMPLIANT WITH JEDEC STANDARD MS-013, VARIATIONS AA, AB, AC, AD & AE.

Lead finish matte Sn: (µm) 8 min/25 max

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	NOTE VARI-ATIONS	3 D MIN.	NOM.	MAX.	5 N
A	.097	.101	.104		AA	.402	.407	.412	16
A_1	.0050	.009	.0115		AB	.451	.456	.461	18
A_2	.090	.092	.094		AC	.500	.505	.510	20
B	.014	.016	.019		AD	.602	.607	.612	24
C	.0091	.010	.0125		AE	.701	.706	.711	28
D	SEE VARIATIONS			3					
E	.292	.296	.299						
e	.050 BSC								
H	.400	.406	.410						
h	.010	.013	.016						
L	.024	.032	.040						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
$α_1$	0°	–	–						
R	.0028	–	–						
R_1	.0028	–	–						
X	.085	.093	.100						

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	NOTE VARI-ATIONS	3 D MIN.	NOM.	MAX.	5 N
A	2.46	2.56	2.64		AA	10.21	10.34	10.46	16
A_1	0.127	0.22	0.29		AB	11.46	11.58	11.71	18
A_2	2.29	2.34	2.39		AC	12.70	12.83	12.95	20
B	0.35	0.41	0.48		AD	15.29	15.42	15.54	24
C	0.23	0.25	0.32		AE	17.81	17.93	18.06	28
D	SEE VARIATIONS			3					
E	7.42	7.52	7.59						
e	1.27 BSC								
H	10.16	10.31	10.41						
h	0.25	0.33	0.41						
L	0.61	0.81	1.02						
N	SEE VARIATIONS			5					
α	0°	5°	8°						
$α_1$	0°	–	–						
R	0.07	–	–						
R	0.07	–	–						
X	2.16	2.36	2.54						

REVISION HISTORY

Revision	Date	Description of Change
1.0	Oct 7, 2013	Initial release
1.1	Oct 21, 2014	Added Reflow Cycle and Moisture Resistance section.
1.2	February 24, 2015	Added matte Sn plating thickness.
2.0	August 6, 2015	Removed 32-SOIC Package. Reference PCN 02895.

CONTACT US

Contact Information:

How to Reach Us:

Home Page:

www.everspin.com

E-Mail:

support@everspin.com

orders@everspin.com

sales@everspin.com

USA/Canada/South and Central America

Everspin Technologies

1347 N. Alma School Road, Suite 220

Chandler, Arizona 85224

+1-877-347-MRAM (6726)

+1-480-347-1111

Europe, Middle East and Africa

support.europe@everspin.com

Japan

support.japan@everspin.com

Asia Pacific

support.asia@everspin.com

EST02614_SOIC Package Guide_Revision2.0 080615

Everspin Technologies, Inc.

Information in this document is provided solely to enable system and software implementers to use Everspin Technologies products. There are no express or implied licenses granted hereunder to design or fabricate any integrated circuit or circuits based on the information in this document. Everspin Technologies reserves the right to make changes without further notice to any products herein. Everspin makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Everspin Technologies assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters, which may be provided in Everspin Technologies data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters including "Typicals" must be validated for each customer application by customer's technical experts. Everspin Technologies does not convey any license under its patent rights nor the rights of others. Everspin Technologies products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Everspin Technologies product could create a situation where personal injury or death may occur. Should Buyer purchase or use Everspin Technologies products for any such unintended or unauthorized application, Buyer shall indemnify and hold Everspin Technologies and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Everspin Technologies was negligent regarding the design or manufacture of the part. Everspin™ and the Everspin logo are trademarks of Everspin Technologies, Inc. All other product or service names are the property of their respective owners.

Copyright © 2014 Everspin Technologies, Inc.